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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,337	08/06/2001	Shunpei Yamazaki	07977-211003	3550

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EXAMINER	
NELSON, ALECIA DIANE	
ART UNIT	PAPER NUMBER
2675	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

TT

Office Action Summary	Application No. 09/924,337	Applicant(s) YAMAZAKI ET AL.	
	Examiner Alecia D. Nelson	Art Unit 2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Priority

1. The statement referencing the priority of the instant application is incorrect. The patent no of U.S. Application No. 08/997, 919 is U.S. Patent No. 6,147,667, opposed to U.S. Patent No. 6,147,919. The error appears to be a typographical error, and the examiner does acknowledge the claim for priority, however it is requested that a corrected statement be submitted in response to the office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

3. ***Claims 1-15, 21-23, and 26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa et al (U.S. Patent No. 5,250,931) in view of Sasaki et al (U.S. Patent No. 5,818,068) and Funai et al. (U.S. Patent No. 5,550,070).

With reference to **claim 1**, Misawa et al. teaches an active matrix panel for driving a liquid crystal display. The active matrix panel includes a plurality of gate lines and source lines and a thin film transistor at each intersection coupled to a liquid crystal driving electrode all formed on a first transparent panel substrate. A second transparent substrate with transparent common electrodes thereon is spaced apart from the panel substrate and a liquid crystal material is placed in the space between the substrates. At least one of a gate line driver circuit and a source line driver circuit is formed on the panel substrate and coupled to the gate lines and source lines. The driver circuits include TFT's of thin film silicon of P-type and N-type (see column 4, line 43-column 5, line 5).

Misawa et al. fails to teach the usage of a logic circuit for processing a signal required for driving the driver circuit and a signal including image information transmitted to the pixel matrix circuit. However, Misawa et al. does teach that the active matrix panel (10) is operated by applying a clock signal CLX and a start signal DX to input terminals (34) and (35) of source line driver circuit (12). A plurality of video signals are input into a plurality of corresponding input terminals (36) of source line driver circuit

(12) (see column 5, lines 6-13). Misawa et al. also fails to teach that the plurality of TFT's comprise a plurality of rod-shaped crystals.

Sasaki et al. teaches an active matrix type display device that includes a negative logic product circuit (13) which has two inputs, and receives logic signals X and Y into input terminals (15) and (16) in synchronization with a clock signal C which is input to a terminal (14) (see column 9, lines 11-19).

Funai et al. teaches that the crystalline silicon region (108) is made of a plurality of needle-shaped or column-shaped silicon crystals having a growth direction in parallel with the surface of the substrate (101) (see column 8, lines 55-58).

With reference to **claims 2-4**, Funai et al. further teaches that in the crystalline silicon film (110), the needle-shaped or column-shaped silicon crystals grow in a direction represented by an arrow (125), and in each needle-shaped or column-shaped silicon crystal, no grain boundaries are present in the direction (125) (see column 10, lines 11-15).

With reference to **claims 5 and 6**, it is an obvious function of liquid crystal devices for there to be an anisotropic property between the channel length direction and a channel width direction of the active layer, as well as there is and intrinsic or substantially intrinsic channel form region of the active layer.

With respects to **claims 7 and 8**, Sasaki et al. teaches that the metal element for enhancing crystallization includes at least one selected from the group consisting of nickel, iron, cobalt, palladium, and platinum. Sasaki et al. fails to teach the specific amount in usage, however the amount of metal element used is designers choice.

With reference to **claim 9**, Funai et al. teaches a gate insulating film (113) is formed on the crystalline silicon film (112), and a gate electrode (114) is formed on the gate insulating film (113). Further it is taught that in the case where the amorphous silicon film (103), the high-concentration nickel region (109), and the region (107) containing nickel in large concentrations are included in the crystalline silicon film (112) (see column 9, lines 45-62).

With respects to **claims 10, 14, and 15**, the usage of plural TFT connecting to each picture element, and the usage of a phase compararator, low pass filter, ect., in a logic circuit, is well known in the art.

With respects to **claims 11-13**, Misawa et al. teaches that a pair of through holes (102) and (103) are opened simultaneously to expose source and drain regions (87) and (89) for connecting conductive line (93) and electrode (94) (see column 22-25). Insulating film (95) acts as a capacitor for preventing application of DC voltages to the liquid crystal material (96) (see column 7, lines 30-35).

With reference to **claims 22 and 26**, it would have been obvious to one having ordinary skill in the art at the time of the invention that the semiconductor device be an electroluminecent device as opposed as an active matrix liquid crystal device being that they are both active matrix and require usage of the same components.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to include a logic circuit as taught by Sasaki et al. to a similar system environment as taught by Misawa et al., this would therefore allow for processing of required driving signals to be transmitted to the pixel matrix via the driving circuit.

4. ***Claims 16-19, 23, and 24*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. in view of Zhang et al. (U.S. Patent No. 5,888,857).

Sasaki et al. teaches a plurality of pixels arranged in a matrix, driver circuitry for driving pixels, and a NAND circuit (13) receives logic signals X and Y into input terminals (15) and (16), which are formed on the dame insulating substrate (see column 5 lines 44-56).

Sasaki et al. fails to teach the sub-threshold coefficients of the transistors, however does teach the usage of the N- and P-type transistors.

Zhang et al. teaches that the field effect mobility of the TFT obtained was 40 to 60 cm^2/Vs in the N channel type and 30 to 500 cm^2/Vs in the P channel type.

With reference to **claims 23 and 24**, it would have been obvious to one having ordinary skill in the art at the time of the invention that the semiconductor device be an electroluminecent device as opposed as an active matrix liquid crystal device being that they are both active matrix and require usage of the same components.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to include the field effect mobility of the TFT's as taught by Zhang et al. to the system as taught by Sasaki et al. to provide and improved semiconductor device with better reliability and performance.

5. ***Claims 20 and 25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. in view of Hirakata (U.S. Patent No. 5,959,599).

Sasaki et al. teaches a plurality of pixels arranged in a matrix, driver circuitry for driving pixels, and a NAND circuit (13) receives logic signals X and Y into input terminals (15) and (16), which are formed on the dame insulating substrate (see column 5 lines 44-56).

Sasaki et al. fails to teach the amount of voltage needed to drive the gate insulating film of the TFT when it is at a certain thickness.

Hirakata teaches an active matrix type liquid-crystal display unit which in the case of using silicon oxide 1200 angstrom in thickness as a gate insulation film, there are very little elements which are destroyed in a stage where a voltage between the gate and the source is up to 10 V (see column 10, lines 29-33). Further it would be obvious to one having ordinary skill in the art to apply a higher operating voltage to the gate insulating film when the film is thicker as opposed to the amount applied when the film is thinner.

With reference to ***claim 25***, it would have been obvious to one having ordinary skill in the art at the time of the invention that the semiconductor device be an electroluminecent device as opposed as an active matrix liquid crystal device being that they are both active matrix and require usage of the same components.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to add the applied voltage levels as taught by Hirakata, to the system as taught by Sasaki et al. to thereby provide an active matrix type liquid crystal display unit in which power consumption is reduced and very little elements are destroyed by applying a higher voltage to the thinner film.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9314 for regular communications and (703)872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-9700.

adn/ADN
April 6, 2003

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
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